

Lattice Gauge Theory and the Computational Physics Department

James N. Simone[†]

Fermi National Accelerator Laboratory

P.O. Box 500

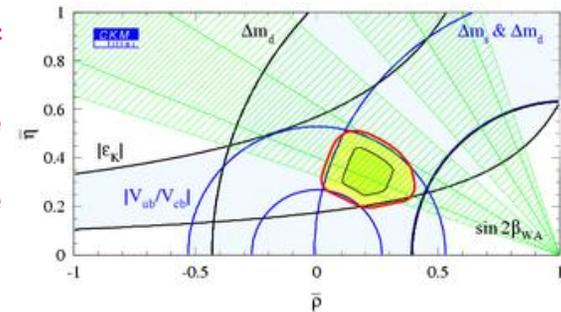
Batavia, IL 60510–0500, USA

CD/CPD – October 2002



Fermilab Lattice QCD and SciDAC

Many important particle physics experiments require lattice gauge theory calculations to interpret them. For example, the parameters describing differences between matter and antimatter shown in the figure can be extracted from Fermilab Tevatron measurements of the properties of B mesons with lattice calculations. The accuracy of these calculations, and therefore of the figure, is likely to improve by an order of magnitude over the next decade.



The DOE SciDAC program funds part of a long-range plan for providing computing infrastructure for the lattice QCD community in the US.

SciDAC@FNAL: commodity cluster construction, network fabric investigations, sys. admin. tools, batch systems, optimized linear alg. kernels, data management, data parallel coding frameworks.



QMP Message Passing API

The SciDAC software committee has designed a communications API specifically for lattice QCD.

- Target NICs able to do memory-to-memory copies with low CPU overhead.
- QCD: Regular patterns of communication among processors, repeated a large number of times.
- Willing to trade slower one-time pattern setup time for very low latency in repeated transfers.
- QMP documents: www.lqcd.org/QMP/

Fermilab will test implementations of QCP for clusters. CPD/ISD/NCSA will provide a testsuite/benchmarks to verify conformance to the API specification and to test performance.



Data management

The SciDAC software committee will develop common formats and interfaces for the manipulation of lattice QCD data and meta-data.

- Binary data standards (single extensible file format, support for legacy formats)
- Meta-data representation (XML?)
- Data storage/retrieval by community
- (Meta-)data replication
- Study EU-datagrid QCDgrid (EPCC) proposals
- QCDgrid documents:
www.ph.ed.ac.uk/ukqcd/community/the_grid/



Custom Prototypes

Currently benchmarking on 3-D torus ($4 \times 5 \times 6$) Athlon cluster in Sweden using commercial Dolphin NICs to investigate parallel scaling of MILC codes on tori.

The Fermilab Electronic Systems Engineering Group is prototyping the Xilinx Virtex-II and Lattice Semiconductor chips for future high-speed DAQ system applications (CKM, BTeV).

ESE will build an additional four Virtex-II prototype cards for lattice QCD.

Features

- four 2.0 Gb/s serial ports
- Cu (Optical) cabling
- 32-bit 33 MHz PCI bus supporting initiator/target block memory moves (DMA)
- rudimentary DMA engine

Investigations: latency, bandwidth, protocol, drivers and QMP implementation



Distribution of CPD Effort

Project	2002	2003
Physics research	0.5	0.5
FNAL Lattice Group support	0.25	0.15
Data management (LGO)	0.10	0.20
QMP (LGO)	0.10	0.05
Custom NIC investigations (LGO)	0.05	0.10

